San Francisco Bay University  
EE461 - Digital Design and HDL

QUIZ 1  
Quiz #1Student Name: Naim Student ID:20176

module mux\_4to1 (out, x0, x1, x2, x3, s0, s1);

input x0, x1, x2, x3; // 4 inputs

input s0, s1; // 2 select signals

output out; // 1 output

wire n\_s0, n\_s1; // Negated select signals

wire p0, p1, p2, p3; // Transmission gate outputs

// Invert the select signals

not (n\_s0, s0);

not (n\_s1, s1);

// Transmission gates for each input based on select lines

assign p0 = (~s1 & ~s0) ? x0 : 1'bz; // Select x0 when s1=0, s0=0

assign p1 = (~s1 & s0) ? x1 : 1'bz; // Select x1 when s1=0, s0=1

assign p2 = (s1 & ~s0) ? x2 : 1'bz; // Select x2 when s1=1, s0=0

assign p3 = (s1 & s0) ? x3 : 1'bz; // Select x3 when s1=1, s0=1

// Combine outputs

assign out = p0 | p1 | p2 | p3;

endmodule

//tb

module test\_mux\_4to1;

reg x0, x1, x2, x3; // 4 inputs

reg s0, s1; // 2 select lines

wire out; // Output wire

// Instantiate the MUX module

mux\_4to1 uut (.out(out), .x0(x0), .x1(x1), .x2(x2), .x3(x3), .s0(s0), .s1(s1));

// Dumping waveform data

initial begin

$dumpfile("dump.vcd"); // Create a VCD file for waveform output

$dumpvars(); // Dump all variables for the entire module

end

// Stimulus block

initial begin

// Apply different input combinations and select lines

$monitor("x0=%b, x1=%b, x2=%b, x3=%b, s0=%b, s1=%b -> out=%b", x0, x1, x2, x3, s0, s1, out);

// Test case 1

x0 = 1; x1 = 0; x2 = 0; x3 = 0; s0 = 0; s1 = 0; #10;

// Test case 2

x0 = 0; x1 = 1; x2 = 0; x3 = 0; s0 = 1; s1 = 0; #10;

// Test case 3

x0 = 0; x1 = 0; x2 = 1; x3 = 0; s0 = 0; s1 = 1; #10;

// Test case 4

x0 = 0; x1 = 0; x2 = 0; x3 = 1; s0 = 1; s1 = 1; #10;

// End simulation

$finish;

end

endmodule

